

Active

Inactive

Active

Inactive

Active

Fig. 1A
(Prior Art)

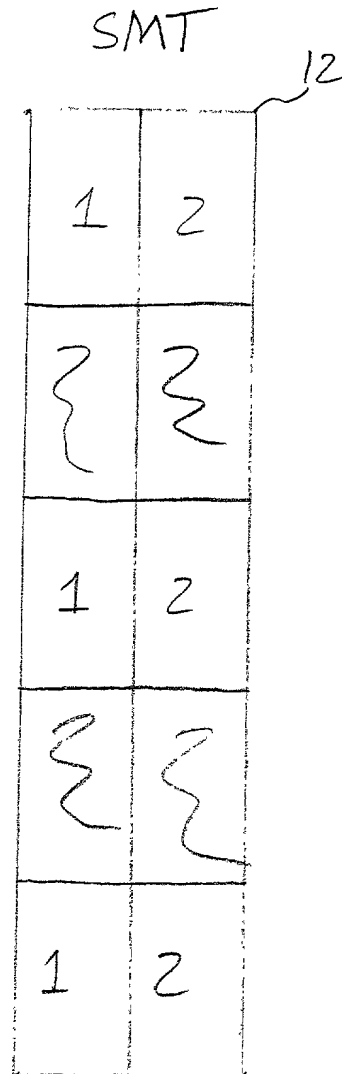


Fig 1B
(Prior Art)

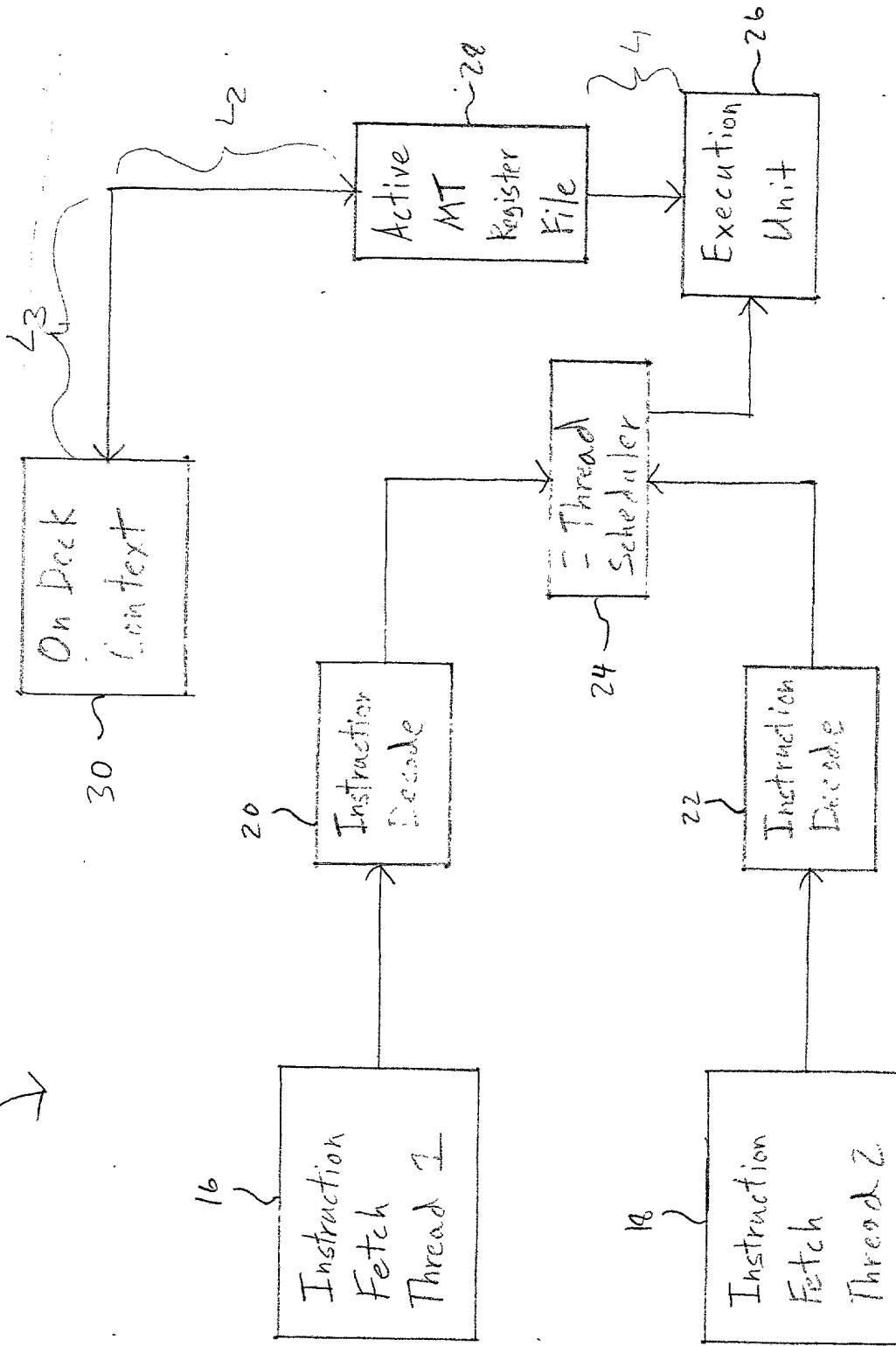


Fig. 2

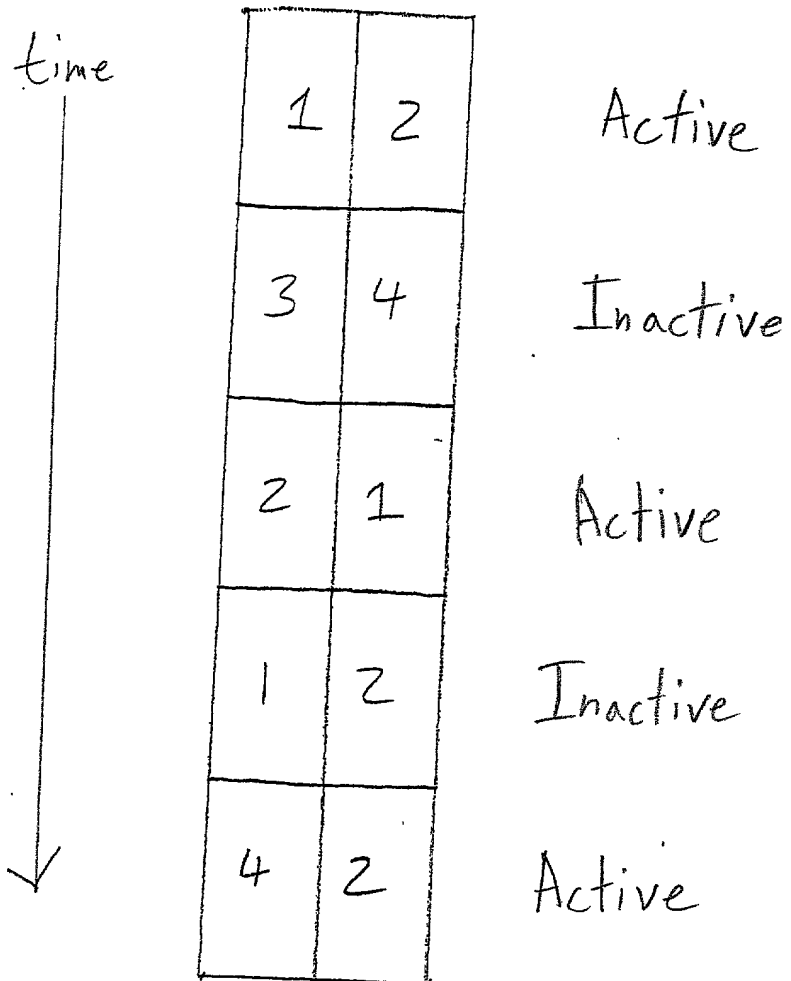


Fig. 3

FIG. 4 is a block diagram of a multi-processor system 32. The system 32 includes four parallel processing units 34, 36, 38, and 40. Each unit 34, 36, 38, and 40 includes an instruction fetch stage, an instruction decode stage, and a 4T SCA stage. The instruction fetch stages 34, 36, 38, and 40 are connected to the instruction decode stages 42, 44, 46, and 48, respectively. The instruction decode stages 42, 44, 46, and 48 are connected to the 4T SCA stage 50. The 4T SCA stage 50 is connected to the execution unit 52. The execution unit 52 is connected to the 4-way MT Register File 54. The 4-way MT Register File 54 is connected to the execution unit 52.

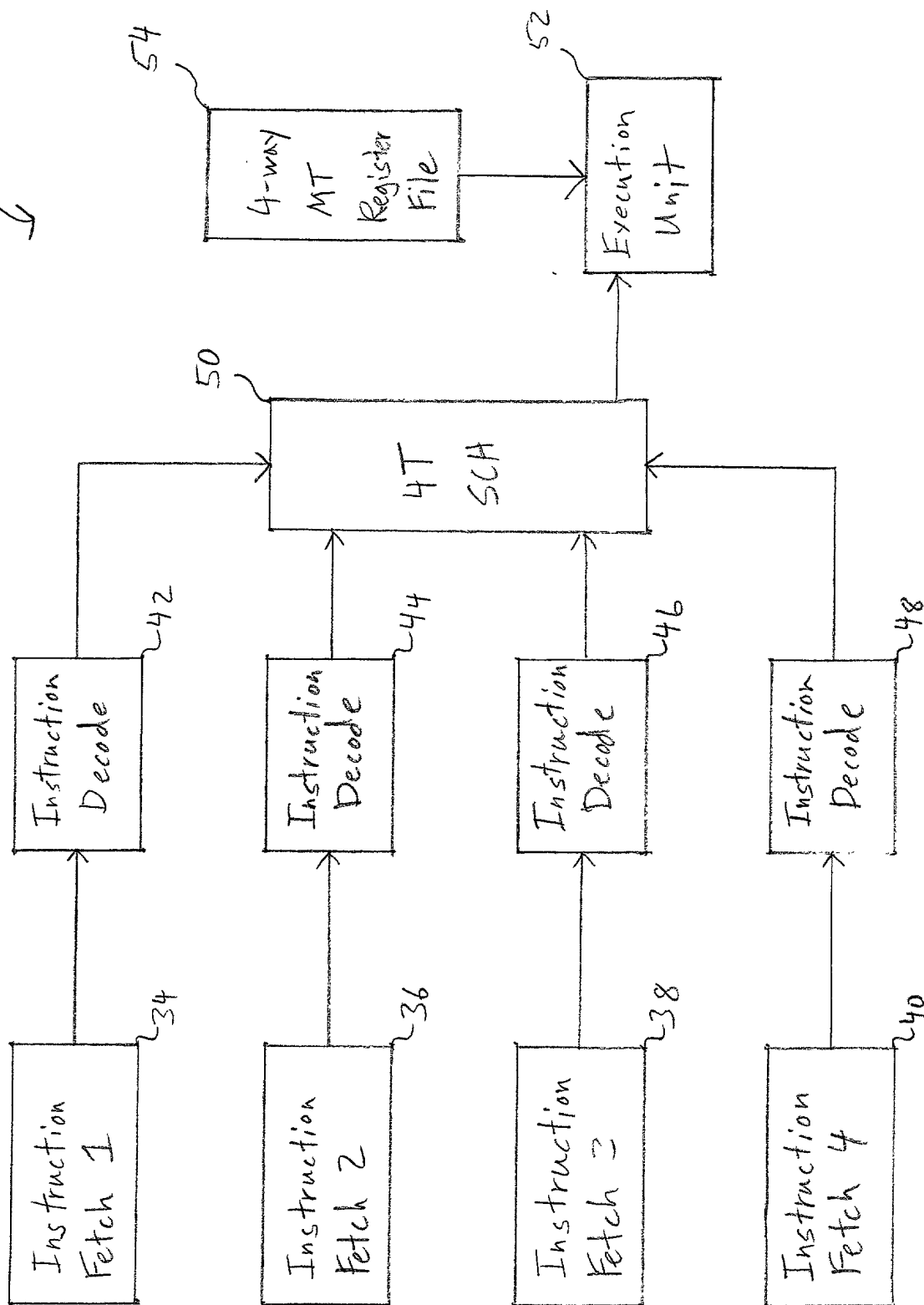


Fig. 4

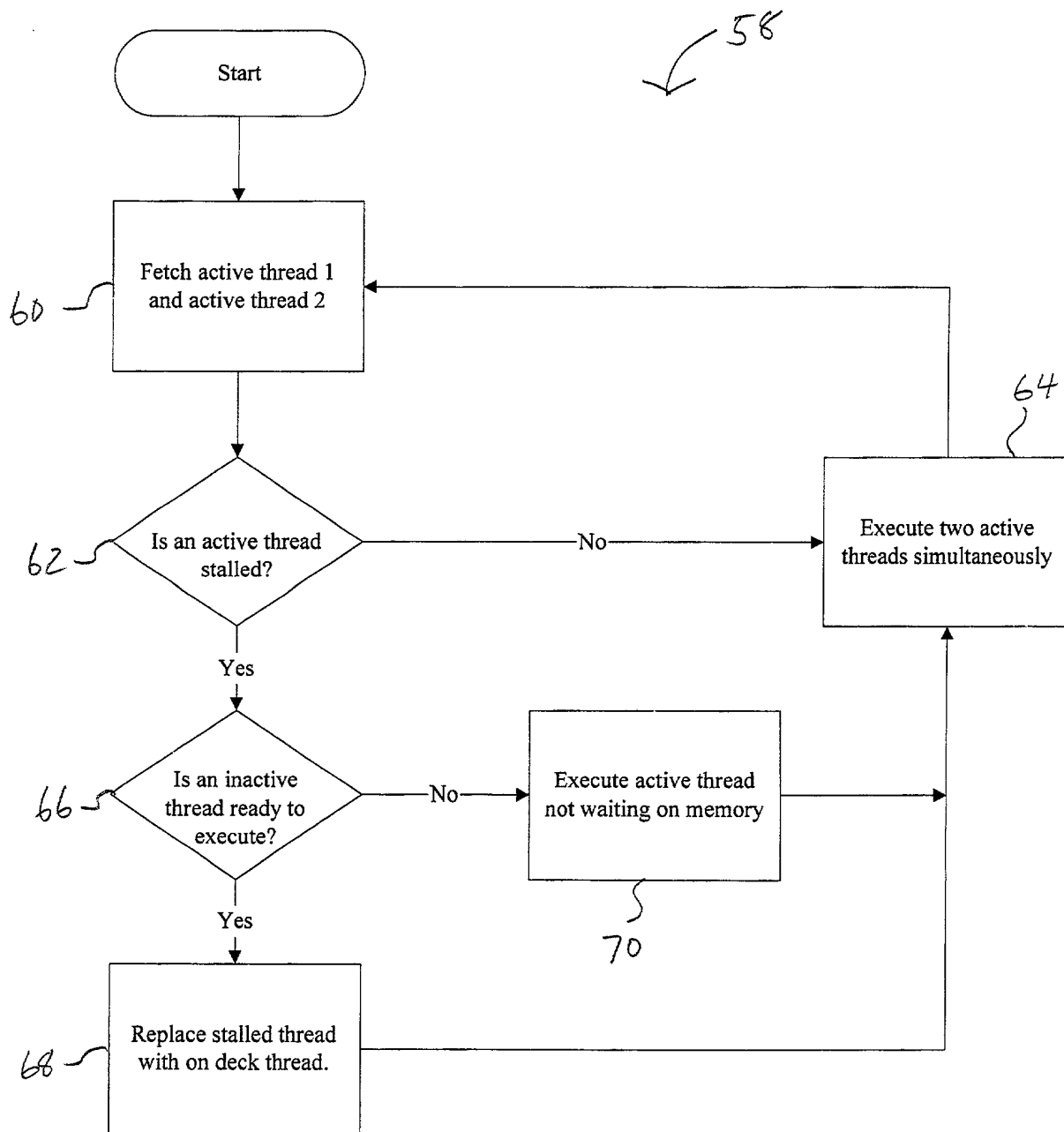


Figure 5